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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,993	01/31/2002	Steven Teig	SPLX.P0100	2856

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,993	TEIG ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *14*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's filing of RCE, amendment, IDS and drawings on 3/15/2004. Claims 1-20 are pending, wherein claims 1,7,12,13 have been amended and claims 15-20 are newly added.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 3/15/2004 has been entered.

Drawings

3. The drawings were received on 3/15/2004. These drawings are acceptable.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. **Claims 1-20** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of copending Application No. 10/066,456. Although the conflicting claims are not identical, they are not patentably distinct from each other because the further limitation that "the at least some of the selected candidate sub-networks having multiple circuit elements that provide multiple outputs of the sub-network" as claimed in the co-pending application is a subset of the candidate sub-networks as claimed in the current application; thus it would have been obvious to one of ordinary skilled in the art at the time of the invention to further apply the methods of claims 1-14 to the particular replacement sub-networks claimed in the co-pending application because the methods of the present application also work for the particular subsets of the replacement sub-networks of the co-pending claims and would further provide greater coverage of the circuits being designed. Furthermore, as per claims 15-16 of the present application, the particular cost function relating to size, timing, or power optimization or combinations thereof as claimed in the present application, would have been obvious to one of ordinary skilled in the at the time of the invention, to further include such cost functions to the co-pending claims since such optimization using cost functions based on size, timing or power is well known in the art and would further provides for the desired design optimizations of the claimed invention. Furthermore, as per claims 17-20 of the present application, the computer readable medium to implement the steps of

claims 1-14 would also have been obvious to one of ordinary skilled in the art at the time of the invention because the methods of claims 1-14 of the present application and the co-pending application are implemented on a computer as further evidence by claim 15 of the co-pending application, and hence the computer implemented methods would necessarily requires the computer readable medium to carry out the methods.

6. **Claims 1-20** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/062,047. Although the conflicting claims are not identical, they are not patentably distinct from each other because the further limitation that "the at least each of a first set of replacement sub-networks having multiple circuit elements, wherein each of the multiple circuit elements of a first-set replacement sub-network is independently selectable by the method" as claimed in the co-pending application is a subset of the candidate sub-networks as claimed in the current application; thus it would have been obvious to one of ordinary skilled in the art at the time of the invention to further apply the methods of claims 1-14 to the particular replacement sub-networks claimed in the co-pending application because the methods of the present application also work for the particular subsets of the replacement sub-networks of the co-pending claims and would further provide greater coverage of the circuits being designed. Furthermore, as per claims 15-16 of the present application, the particular cost function relating to size, timing, or power optimization or combinations thereof as claimed in the present application, would have been obvious to one of ordinary skilled in the at the time of the invention, to further include such cost functions to the co-pending claims

since such optimization using cost functions based on size, timing or power is well known in the art and would further provides for the desired design optimizations of the claimed invention. Furthermore, as per claims 17-20 of present application, the computer readable medium to implement the steps of claims 1-14 would also have been obvious to one of ordinary skilled in the art at the time of the invention because the methods of claims 1-14 of the present application and the co-pending application are implemented on a computer, and hence the computer implemented methods would necessarily requires the computer readable medium to carry out the methods.

7. **Claims 1-20** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/061,719. Although the conflicting claims are not identical, they are not patentably distinct from each other because the further limitation that "the at least some of the selected candidate sub-networks having a graph structure that is different from a tree structure or a micro-leaf directed acyclic graph structure" as claimed in the co-pending application is a subset of the candidate sub-networks as claimed in claims 1-14 in the current application; thus it would have been obvious to one of ordinary skilled in the art at the time of the invention to further apply the methods of claims 1-14 to the particular replacement sub-networks claimed in the co-pending application because the methods of the present application also work for the particular subsets of the replacement sub-networks of the co-pending claims and would further provide greater coverage of the circuits being designed. Furthermore, as per claims 15-16 of the present application, the particular cost function relating to size, timing, or

power optimization or combinations thereof as claimed in the present application, would have been obvious to one of ordinary skilled in the at the time of the invention, to further include such cost functions to the co-pending claims since such optimization using cost functions based on size, timing or power is well known in the art and would further provides for the desired design optimizations of the claimed invention. Furthermore, as per claims 17-20 of the present application, the computer readable medium to implement the steps of claims 1-14 would also have been obvious to one of ordinary skilled in the art at the time of the invention because the methods of claims 1-14 of the present application and the co-pending application are implemented on a computer as further evidenced by claim 14 of the co-pending application, and hence the computer implemented methods would necessarily requires the computer readable medium to carry out the methods.

8. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 1-6,17-20** are rejected under 35 U.S.C. 102(e) as being anticipated by **Cirit** (US Patent No. 6,523,156).

As per **claims 1,6,17**, all of the elements of the claims are illustrated in Figs. 3 and 4 (see also col. 5, line 55 to col. 9, line 50), wherein the mapping into the technology is done as part of steps 304-316, wherein the repetitive steps of selecting/identifying/replacing are done as part of the constant replacement delay cell library (blocks 350 and 314) which are illustrated in Fig. 4, performed in iterative/repetitive manner until the stopping criteria is reached, wherein the candidate sub-network corresponds to the cell identified for replacement, and the storage structure corresponds to the cell library, wherein prior to synthesis, these circuit descriptions are not bound to a particular technology (see col. 7, line 56 to col. 87, line 12) wherein the computer readable medium having program is described in col. 11, line 65 to col. 12, line 11.

As per **claims 2-3**, the parameter generation and retrieval of the sub-network (e.g., replacement cell) from the storage structure (e.g., library) is also part of steps 404-406, wherein at least the load is being used as the parameter calculated/generated to retrieval the proper replacement from the library.

As per **claims 4-5**, the set of output functions being one or more output functions is also part of the method/system since one or more cells or combinations thereof which

inherently have correspond one or more outputs, are being replaced (see col. 7, lines 28-42).

As per **claims 18-20**, all of the elements of claim 17, which the claims depend, are discussed in the rejection of claims 17 above, wherein the further limitation in which evaluation for replacing the sub-network (e.g., replacement cells) performed including based on costs or constraints or combined costs, relating to sizing, timing, or power consumption, are further described in col. 7, lines 1-42 and col. 8, lines 13-45, wherein such combined constraints or costs (i.e., taking power, load, and timings into consideration) are further described in col. 12, line 48 to col. 13, line 26.

11. **Claims 1-20** are rejected under 35 U.S.C. 102(b) as being anticipated by **Damiano et al.** (US Patent No. 5,537,330).

Damiano et al. disclose a method/system within a logic synthesis system which provides for using tags attached to the nodes of the circuit abstraction (e.g., technology independent description--design not bound to a particular technology) to separately map and optimize the design into the specific technology based on the particular mode (open control, structure dominant or direct map) (see abstract).

As per **claims 1,6,17**, all of the elements of the claims are illustrated in Figs. 1-4, wherein as shown in Fig. 1, design not bound to the particular technology (i.e., technology independent) corresponds to block 105, which is mapped into the particular technology 113 using blocks 107-111, wherein such mapping is performed separately from unbounded technology design for each mode (e.g., open control, structure dominant, or direct map--see col. 6, line 44 to col. 7, line 67), wherein as further

illustrated in Figs. 3 and 4, the mapping and optimizing (for structure dominance and direct mapping modes) involves repeated loops (e.g., 403-423 in Fig. 3 and 503-523 in Fig. 4) involving selection (401, 501 in Figs. 3 and 4 respectively), identification (403-431,503-505 in Figs. 3 and 4 respectively) and replacement (429, 507 in Figs. 3 and 4 respectively), including until the stopping criteria is reached at least corresponds to blocks 423 and 511 of Figs. 3 and 4 respectively, wherein since the system/method is computer-implemented system/method (col. 1-2), the computer readable medium and programs stored thereon are inherently included as being necessary to implement the method/system.

As per **claims 2-3**, the parameter generation and retrieval of the sub-network (e.g., replacement cell) from the storage structure (e.g., library) are part of the attributes or constraints generated in order for the covering algorithm to properly optimize and map/replace the sub-networks to the specific technology (see col. 9, lines 10-25; col. 9, line 56 to col. 10, line 4).

As per **claims 4-5**, the set of output functions being one or more output functions is also part of the method/system since one or more cells or combinations thereof are discussed in col. 7, lines 30-62.

As per **claims 7-13,18**, the further traversing of the design after the terminating repetitions (e.g., at least in block 511 which transfer to structure dominance processing block 515 of Fig. 4) are further described in Fig. 3, in which the various sub-networks are identified, evaluated, and matched, wherein the evaluations before replacing the

candidate sub-network is part of the matching procedures (e.g., 405, 431, 411, 415, 427 of Fig. 3 and 505, 511 of Fig. 4).

As per **claims 14-16,19-20**, the evaluation based on cost function including timing, size, or power consumption or combinations thereof, are further described in col. 10, lines 55-67 as part of the attributes affecting the modes (i.e., at least direct mapping mode used to control the particular matching/mapping of Fig. 4).

Remarks

12. The allowance of claims 1-14 are withdrawn due to Applicant's amendment to the independent the claims, which are not patentable over the prior arts as given in the rejections above.

13. As per claims 15-20, the claims are newly rejected as given above, as being necessitated by Applicant's addition of the claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicants are herein requested to consider them carefully in response to this Office Action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(571) 273-1895 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing).

16. **Applicant should note that effective May 1, 2003, the United States Patent and Trademark Office has a new Commissioner for Patents address for transitioning to the new Office location in Alexandria, VA, wherein**

correspondence in patent-related matters to organizations reporting to the Commissioner for Patents must now be addressed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

VUTHE SIEK
PRIMARY EXAMINER

PK
May 1, 2004